On the Energy and Performance of Commodity Hardware Transactional Memory

Nuno Diegues and Paolo Romano and Luís Rodrigues

Transactional Memory (TM)
- multi-core processors are standard
- locking approaches are complex
- TM is an abstraction for synchronization
- programmers identify atomic blocks
- runtime implements the synchronization

Now also in hardware: x86 extensions in Intel Core processors with Transactional Synchronization Extensions (TSX)
- traditional, pessimistic approach
- requires per-application effort
- synchronization in hardware is efficient but limited, not suited for all workloads
- transactions may abort due to:
  - forbidden instructions
  - capacity of L1 cache
  - faults and signals
  - (besides contention to data)

Research question: how does commodity HTM fare against existing available alternatives?

Software TMs (4 impls)
- instrumented reads and writes
- software runtime validates transactions
  - easy prototyping, robust implementations
  - overhead of software concurrency control

Hybrid TMs (2 impls)
- use STM on fallback of HTM
- long, conflicting txs use STM
- best of both worlds?
  - complex integration of strategies

Locks (6 impls)
- traditional, pessimistic approach
- requires per-application effort
- can be highly optimised

STM is still competitive
- despite commodity hardware
- best STM was better than HTM in 71% of the scenarios

Hybrid TMs inherit worst of both worlds
- never the best approach in any scenario

Summary of results
- 560 scenarios using TM standard benchmarks

<table>
<thead>
<tr>
<th>Transactionality (%)</th>
<th>Speedup</th>
<th>Least Energy</th>
</tr>
</thead>
<tbody>
<tr>
<td>kmeans low (7)</td>
<td>HTM</td>
<td>HTM</td>
</tr>
<tr>
<td>low (17)</td>
<td>HTM</td>
<td>HTM</td>
</tr>
<tr>
<td>intruder medium (33)</td>
<td>HTM ≤ 4t</td>
<td>HTM ≤ 5t</td>
</tr>
<tr>
<td>vacation medium (89)</td>
<td>STG ≥ 5t</td>
<td>STG ≥ 6t</td>
</tr>
<tr>
<td>genome high (97)</td>
<td>HTM ≤ 2t</td>
<td>STG ≤ 4t</td>
</tr>
<tr>
<td>yada high (99)</td>
<td>STG ≥ 3t</td>
<td>STG ≥ 5t</td>
</tr>
<tr>
<td>labyrinth high (100)</td>
<td>STM</td>
<td>STM</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hash Map 10% writes</th>
<th>Red-Black Tree 90% writes</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTM</td>
<td>Fine-Locks</td>
</tr>
<tr>
<td>STG</td>
<td>STM</td>
</tr>
</tbody>
</table>

Research Directions

Selective Instrumentation
- 20% impact on STM and Hybrid approaches

Tuning HTM
- optimal configuration
- up to 80% better than best configuration on average

Selective Instrumentation
- manual compiler

This work was supported by PEst-OE/EEI/LA0021/2013 from Fundação para a Ciência e Tecnologia in Portugal and by the GreenTM project (EXPL/EEI-ESS/0361/2013).